U.S. UTILITY Patent Application

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PATENT NUMBER and ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10021497	12/19/2001	257	374	2811	2822 Sim T. Chan

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**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB DO NOT PUBLISH ☐ RESCIND ☐

Foreign priority claimed ☐ yes ☐ no
35 USC 119 conditions met ☐ yes ☐ no
Verified and Acknowledged Examiners's initials

ATTORNEY DOCKET NO
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TITLE : Array of gate dielectric structures to measure gate dielectric thickness and parasitic capacitance

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED: Total Claims	Print Claim for O.G
ISSUE FEE: Amount Due	Date Paid	Primary Examiner	DRAWING: Sheets Drwg.	Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAMER		PREPARED FOR ISSUE	Application Examiner	

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